EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	186	(712/238).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 15:37
L2	278	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 15:37
L3	4	((branch$3 with ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 with stall$3)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 15:38
L4	1	((branch$3 with ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 with stall$3)).clm.	US-PGPUB	OR	OFF	2006/04/17 15:38
L5	1	(vliw with (branch with (slot$1 or entr$3))).clm.	US-PGPUB	OR	OFF	2006/04/17 15:41
L6	1	(vliw same (branch same ((slot$1 or entr$3) with ((instruction$1 or prefetch$3) with (buffer$1 or cache$1))))).clm.	US-PGPUB	OR	OFF	2006/04/17 15:41
L7	2	((branch$3 same ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 with stall$3)).clm.	US-PGPUB	OR	OFF	2006/04/17 15:41
L8	2	((branch$3 same ((target or address or location) same (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 same stall$3)).clm.	US-PGPUB	OR	OFF	2006/04/17 15:41
L9	22	((branch$3 with ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 with stall$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/17 15:38
L10	7	((branch$3 with ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 with stall$3))	US-PGPUB	OR	OFF	2006/04/17 15:39
L11	3	(vliw with (branch with (slot$1 or entr$3)))	US-PGPUB	OR	OFF	2006/04/17 15:41
L12	1	(vliw same (branch same ((slot$1 or entr$3) with ((instruction$1 or prefetch$3) with (buffer$1 or cache$1)))))	US-PGPUB	OR	OFF	2006/04/17 15:41

L13	20	((branch$3 same ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 with stall$3))	US-PGPUB	OR	OFF	2006/04/17 15:41
L14	51	((branch$3 same ((target or address or location) same (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 same stall$3))	US-PGPUB	OR	OFF	2006/04/17 15:41
S1	167	(712/238).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 07:56
S2	252	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/04/29 15:29
S3	2	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3))) near4 (pipelin$3 near4 stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:06
S4	20	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 near4 stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:31
S5	3	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 near4 stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/04/29 15:37
S6	173	(712/238).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:05
S7	257	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:05
S8	5	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 near4 stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:06
S9	17	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3))) with (stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:06
S10	1	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3)) near4 (allocat$3 or assign$3 or mak$3 or creat$3)) with (stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:07

S11	2	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3)) near4 (allocat$3 or assign$3 or mak$3 or creat$3)) same (stall$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:08
S12	89	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3)) near4 (allocat$3 or assign$3 or mak$3 or creat$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:08
S13	1	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3)) near4 (allocat$3 or assign$3 or mak$3 or creat$3)) with (prefetch$3 adj1 (buffer$1 or cach$3 or memor$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:10
S14	4	(branch$3 near4 ((target or address or location) adj2 (buffer$1 or cache$1 or tabl$3)) near4 (allocat$3 or assign$3 or mak$3 or creat$3)) same (prefetch$3 adj1 (buffer$1 or cach$3 or memor$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/12 14:10
S15	8	(prefetch$3 near4 buffer$3) near4 ((branch$3 or jump$3) near4 (slot$1 or entr$3 or position$1 or area$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 08:05
S16	12	(prefetch$3 near4 buffer$3) with ((branch$3 or jump$3) near4 (slot$1 or entr$3 or position$1 or area$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 08:07
S17	47	(prefetch$3 near4 buffer$3) same ((branch$3 or jump$3) near4 (slot$1 or entr$3 or position$1 or area$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 08:09
S18	9	vliw near4 (branch near4 (slot$1 or entr$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:32
S19	1	vliw with (branch near4 (slot$1 or entr$3) near4 ((instruction$1 or prefetch$3) near4 (buffer$1 or cache$1)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 10:37
S20	1	vliw same (branch near4 (slot$1 or entr$3) near4 ((instruction$1 or prefetch$3) near4 (buffer$1 or cache$1)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 10:37
S21	1	vliw same (branch with ((slot$1 or entr$3) near4 ((instruction$1 or prefetch$3) near4 (buffer$1 or cache$1))))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 10:38

S22	1	vliw same (branch same ((slot$1 or entr$3) near4 ((instruction$1 or prefetch$3) near4 (buffer$1 or cache$1))))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 10:38
S23	2	vliw same (branch same ((slot$1 or entr$3) with ((instruction$1 or prefetch$3) with (buffer$1 or cache$1))))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:33
S24	2	(("6154833") or ("5996071")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 10:59
S25	174	(712/238).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 11:06
S26	257	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/25 11:06
S27	7	(US-5701448-$ or US-5835754-$ or US-6216219-$ or US-6308322-$ or US-6157988-$ or US-6029228-$ or US-5909566-$).did.	USPAT	OR	OFF	2005/07/25 12:03
S28	183	(712/238).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:27
S29	271	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:27
S30	5	(("5477640") or ("6308322") or ("6157988") or ("5909566") or ("5701448")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:28
S31	5	(("6477640") or ("6308322") or ("6157988") or ("5909566") or ("5701448")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:28
S32	4	((branch$3 with ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 with stall$3)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/12/21 15:32
S33	1	((branch$3 with ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) with (pipelin$3 with stall$3)).clm.	US-PGPUB	OR	OFF	2005/12/21 15:33

S34	1	(vliw with (branch with (slot$1 or entr$3))).clm.	US-PGPUB	OR	OFF	2005/12/21 15:33
S35	1	(vliw same (branch same ((slot$1 or entr$3) with ((instruction$1 or prefetch$3) with (buffer$1 or cache$1))))).clm.	US-PGPUB	OR	OFF	2005/12/21 15:33
S36	2	((branch$3 same ((target or address or location) with (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 with stall$3)).clm.	US-PGPUB	OR	OFF	2005/12/21 15:34
S37	2	((branch$3 same ((target or address or location) same (buffer$1 or cache$1 or tabl$3))) same (pipelin$3 same stall$3)).clm.	US-PGPUB	OR	OFF	2005/12/21 15:34

Google Scholar BETA

Scholar Results **1 - 10** of about **381** for **branch prediction + prefetch buffer + slot**. (2.33 seconds)

Reducing the **Branch** Penalty in Pipelined Processors - group of 6 »
DJ Lilja - IEEE Computer, 1988 - doi.ieeecomputersociety.org
... costs, and the real performance cost of an incorrect **prediction**. **Branch** target **buffer** ...
prefetched from the sequential instruction stream into a **prefetch buffer**. ...
Cited by 54 - Web Search

AMULET3 Revealed - group of 7 »
JD Garside, SB Furber, SH Chung - target - doi.ieeecs.org
... Thumb instruction at the lower address) **prediction** because this ... not be accepted
immediately by the **prefetch** unit and instructions in the **branch** shadow must ...
Cited by 38 - Web Search

POWER4 system microarchitecture - group of 45 »
JM Tendler, JS Dodson, JS Fields, H Le, B Sinharoy - IBM JOURNAL OF RESEARCH AND
DEVELOPMENT, 2002 - research.ibm.com
... Using the **branch-prediction** logic, the IFAR is reloaded and ... are stored in the
instruction-**prefetch buffer** so that ... oldest instruction is placed in **slot** 0, the ...
Cited by 170 - Cached - Web Search - BL Direct

An Evaluation of **Branch** Architectures - group of 2 »
JA DeRosa, HM Levy - ISCA, 1987 - portal.acm.org
... performance im- provement such as **branch prediction** and prefetching. ... the **branch**-taken
and **branch**-not-taken ... With the second **prefetch buffer**, the one-instruction ...
Cited by 27 - Web Search

Portable Execution Time Analysis for RISC Processors - group of 3 »
K Narasimhan, KD Nilsen - ACM SIGPLAN Workshop on Language, Compiler and Tool Support ...,
1994 - cc.gatech.edu
... among the analytical timing **prediction** schemes that ... point Unit (FPU) and **Branch**
Processing Unit ... in the four-**slot** instruction **prefetch buffer** leapfrogs directly ...
Cited by 30 - View as HTML - Web Search

Branch target **buffer** design and optimization - group of 5 »
CH Perleberg, AJ Smith - IEEE Transactions on Computers, 1993 - ieeexplore.ieee.org
... the penalty of a wrong **branch prediction**, both paths of ... the occurrence of still another
branch before a ... **Prefetch Branch** Target: Most computers follow the fall ...
Cited by 82 - Web Search - Library Search - BL Direct

Advanced Performance Features of the 64-bit PA-8000 - group of 5 »
D Hunt - COMPCON, 1995 - ieeexplore.ieee.org
... while programs which have not been profiled use dynamic **prediction**. ... cycle in the
rare event of a mis- predicted **branch**. ... with a **slot** of the memory **buffer** in the ...
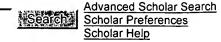Cited by 106 - Web Search - BL Direct

Hardware support for hiding cache latency - group of 3 »
M Golden, TN Mudge - 1993 - eecs.umich.edu
... Imperfect **branch prediction** could decrease performance because the ... from an instruction

Google Scholar™ BETA

branch prediction + prefetch buffer + entry   [Search]

Scholar Results 1 - 10 of about **1,110** for **branch prediction + prefetch buffer + entry**. (2.49 seconds)

An effective on-chip preloading scheme to reduce data access penalty - group of 3 »
JL Baer, TF Chen - SC, 1991 - portal.acm.org
... If some form of **branch prediction** mechanism is ... "ahead" of the functional stream and
hence **prefetch** ... based on sequentiality (OBL, I-stream **buffer**) can be ...
Cited by 219 - Web Search - Library Search

Reducing Memory Latency via Non-blocking and F% efetching Caches - group of 7 »
TF Chen, JL Baer - portal.acm.org
... bytes data cache[I]. **Branch prediction** is performed ... two- bit state transition **Branch**
Target **Buffer** ... tech- niques, including prefetching caches (**PREFETCH**), write ...
Cited by 154 - Web Search - Library Search - BL Direct

POWER4 system microarchitecture - group of 45 »
JM Tendler, JS Dodson, JS Fields, H Le, B Sinharoy - IBM JOURNAL OF RESEARCH AND
DEVELOPMENT, 2002 - research.ibm.com
... earlier, for cases in which the **branch-prediction** logic is in error, the
branch-execution unit ... into one **entry** of the instruction-**prefetch buffer** so that the ...
Cited by 170 - Cached - Web Search - BL Direct

Reducing the **Branch** Penalty in Pipelined Processors - group of 6 »
DJ Lilja - IEEE Computer, 1988 - doi.ieeecomputersociety.org
... and the real performance cost of an incorrect **prediction**. ... When a nonsequential **branch**
occurs, however, the required ... most likely is not in the **prefetch buffer**. ...
Cited by 54 - Web Search

Data **prefetch** mechanisms - group of 9 »
SP Vanderwiel, DJ Lilja - ACM Computing Surveys, 2000 - portal.acm.org
Page 1. Data **Prefetch** Mechanisms ... Many of these cache misses can be avoided if we
augment the demand fetch policy of the cache with a data **prefetch** operation. ...
Cited by 68 - Web Search - BL Direct

Two Techniques to Enhance the Performance of Memory Consistency Models - group of 4 »
K Gharachorloo, A Gupta, JL Hennessy - ICPP (1), 1991 - csl.cornell.edu
... can be retired from this **buffer** as fast ... that has dynamic scheduling and **branch**
prediction capability. As with **prefetch**- ing, the speculative technique also ...
Cited by 92 - View as HTML - Web Search

Predictor-directed stream buffers - group of 18 »
T Sherwood, S Sair, B Calder - MICRO-ANNUAL WORKSHOP THEN ANNUAL INTERNATIONAL
SYMPOSIUM-, 2000 - portal.acm.org
... This is accomplished by decoupling the **branch** predictor from the instruction cache
with a ... stream **buffer entry** is freed for a new **prediction** and **prefetch**. ...
Cited by 48 - Web Search - BL Direct

Dead-block **prediction** & dead-block correlating prefetchers - group of 15 »
AC Lai, C Fide, B Falsafi - ACM SIGARCH Computer Architecture News, 2001 -
doi.ieeecomputersociety.org
... Much as two-level **branch** predictors, the miss address ... an L1 miss incurring high **prefetch**
hit latency. ... correlation alone results in low **prediction** accuracy and ...

Google Scholar BETA

Scholar Results **1 - 10** of about **744** for **branch prediction + prefetch buffer + location**. (2.23 seconds)

Reducing the **Branch** Penalty in Pipelined Processors - group of 6 »
DJ Lilja - IEEE Computer, 1988 - doi.ieeecomputersociety.org
... costs, and the real performance cost of an incorrect **prediction**. **Branch** target **buffer** ...
prefetched from the sequential instruction stream into a **prefetch buffer**. ...
Cited by 54 - Web Search

Single instruction stream parallelism is greater than two - group of 5 »
M Butler, TY Yeh, Y Patt, M Alsup, H Scales, M ... - ACM SIGARCH Computer Architecture News, 1991 -
portal.acm.org
... niscient, **branch prediction** and unbounded functional units, is not realizable.
Nonetheless several variations of the RDF model are interesting to study. ...
Cited by 109 - Web Search

An effective on-chip preloading scheme to reduce data access penalty - group of 3 »
JL Baer, TF Chen - SC, 1991 - portal.acm.org
... If some form of **branch prediction** mechanism is ... "ahead" of the functional stream and
hence **prefetch** ... based on sequentiality (OBL, I-stream **buffer**) can be ...
Cited by 219 - Web Search - Library Search

AMULET3 Revealed - group of 7 »
JD Garside, SB Furber, SH Chung - target - doi.ieeecs.org
... Thumb instruction at the lower address) **prediction** because this ... not be accepted
immediately by the **prefetch** unit and instructions in the **branch** shadow must ...
Cited by 38 - Web Search

Two Techniques to Enhance the Performance of Memory Consistency Models - group of 4 »
K Gharachorloo, A Gupta, JL Hennessy - ICPP (1), 1991 - csl.cornell.edu
... can be retired from this **buffer** as fast ... beneficial for hardware-controlled **prefetch**
schemes. ... **Branch prediction** techniques that allow execution of instructions ...
Cited by 92 - View as HTML - Web Search

[PS] Speculative Execution via Address **Prediction** and Data Prefetching - group of 14 »
J Gonzalez, A Gonzalez - International Conference on Supercomputing, 1997 - ac.upc.edu
... request **buffer** that will keep **prefetch** request until a memory port is available.
Effe. Add. Stride SHB Value V DR DI + Value OK? ... **Branch prediction** is ...
Cited by 91 - View as HTML - Web Search

POWER4 system microarchitecture - group of 45 »
JM Tendler, JS Dodson, JS Fields, H Le, B Sinharoy - IBM JOURNAL OF RESEARCH AND
DEVELOPMENT, 2002 - research.ibm.com
... lines are stored in the instruction-**prefetch buffer** so that ... a store to the memory
location from another ... to the instruction-fetching and **branch-prediction** cycles ...
Cited by 170 - Cached - Web Search - BL Direct

Characterization of database access pattern for analytic **prediction** of **buffer** hit probability - group of 5 »
A Dan, PS Yu, JY Chung - The VLDB Journal The International Journal on Very Large ..., 1995 - Springer
... Therefore, each **branch** record is accessed more often ... components for use in future
buffer hit **prediction**. ... a large enough NT to avoid substantial false **prefetch** ...